This listing of claims will replace all prior versions, and listings, of claims in the present application.

LISTING OF CLAIMS:

Claim 1 (Currently Amended) A semiconductor IC structure comprising:

a semiconductor substrate including at least one front-end-of-the-line device (FEOL) located on a surface thereof;

at least one metal resistor located on, or in close proximity to, said surface of said semiconductor substrate, said at least one metal resistor comprising at least a conductive metal; and

a first level of metallization above said at least one metal resistor.

Claim 2 (Currently Amended) The semiconductor IC structure of Claim 1 further comprising a trench isolation region in said semiconductor substrate, and said at least one metal resistor is positioned on said trench isolation region.

Claim 3 (Original) The semiconductor IC structure of Claim 1 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

Claim 4 (Original) The semiconductor IC structure of Claim 3 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

Claim 5 (Original) The semiconductor IC structure of Claim 1 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 6 (Original) The semiconductor IC structure of Claim 1 further comprising an etch stop layer located beneath said conductive metal.

Claim 7 (Original) The semiconductor IC structure of Claim 6 wherein said etch stop layer has a thickness from about 20 to about 50 nm.

Claim 8 (Currently Amended) The semiconductor IC structure of Claim 1 further comprising a dielectric material on said at least one metal resistor.

Claim 9 (Original) The semiconductor IC structure of Claim 1 wherein said first level of metallization comprises an interlevel dielectric material having contact openings that are filled with a conductive material.

Claim 10 (Original) The semiconductor IC structure of Claim 1 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

Claim 11 (Withdrawn) A method for integrating a metal resistor into a CMOS technology comprising the steps of:

forming at least one FEOL device on a surface of a semiconductor substrate;

forming at least one resistor on, or in close proximity to, the surface of said semiconductor substrate, said at least one resistor comprising a conductive metal; and

forming a first level of metallization over said semiconductor structure.

Claim 12 (Withdrawn) The method of Claim 11 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

Claim 13 (Withdrawn) The method of Claim 11 wherein said semiconductor substrate includes a trench isolation region and said at least one resistor is formed thereon.

Claim 14 (Withdrawn) The method of Claim 11 wherein said forming said at least one resistor comprises forming an etch stop layer over said at least one FEOL device; forming a conductive metal on said etch stop layer; forming a dielectric material on said conductive metal; and patterning said conductive metal and said dielectric material to provide a stack including said conductive metal and said dielectric material

Claim 15 (Withdrawn) The method of Claim 11 wherein said forming said at least one resistor comprises providing a planarized dielectric material on said surface of said semiconductor substrate including said at least one FEOL device; forming a conductive metal on

said planarized dielectric material; forming a dielectric material on said conductive metal; and patterning said conductive metal and said dielectric material to provide a stack.

Claim 16 (Withdrawn) The method of Claim 11 wherein said forming said at least one resistor comprises forming a silicide metal layer over said semiconductor substrate including said at least one FEOL device; forming a dielectric material over said silicide metal layer; patterning said dielectric material and said silicide metal layer to provide at least one stack on said surface of said semiconductor substrate; and annealing to convert the silicide metal layer of said stack into a metal silicide, wherein said metal silicide of said stack comprises a conductor of a resistor

Claim 17 (Withdrawn) The method of Claim 11 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

Claim 18 (Withdrawn) The method of Claim 17 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

Claim 19 (Withdrawn) The method of Claim 11 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 20 (Withdrawn) The method of Claim 11 wherein said forming said first level of metallization comprises forming an interlevel dielectric material; providing contact openings in said interlevel dielectric; and filling said contact openings with a conductive metal.

Claim 21 (Withdrawn) A method for integrating a metal resistor into a CMOS technology comprising the steps of:

providing a structure including at least one FEOL device located on a surface of a semiconductor substrate;

forming an etch stop layer over said structure including said at least one FEOL device;

forming a conductive metal on said etch stop layer;

forming a dielectric material on said conductive metal;

patterning said conductive metal and said dielectric material to provide a stack including said conductive metal and said dielectric material; and

forming a first level of metallization over said at least one FEOL device and said stack.

Claim 22 (Withdrawn) The method of Claim 21 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

Claim 23 (Withdrawn) The method of Claim 21 wherein said semiconductor substrate includes a trench isolation region and said at least one resistor is formed thereon.

Claim 24 (Withdrawn) The method of Claim 21 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, or SiCr.

Claim 25 (Withdrawn) The method of Claim 24 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

Claim 26 (Withdrawn) The method of Claim 21 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 27 (Withdrawn) The method of Claim 21 wherein said etch stop layer has a thickness from about 20 to about 50 nm.

Claim 28 (Withdrawn) A method for integrating a metal resistor into a CMOS technology comprising the steps of:

providing a structure including a planarized dielectric material located on a surface of a semiconductor substrate that comprises at least one FEOL device located thereon;

forming a conductive metal on said planarized dielectric material;

forming a dielectric material on said conductive metal;

patterning said conductive metal and said dielectric material to provide a stack; and

forming a first level of metallization over at least said stack, said planarized dielectric and said at least one FEOL device.

Claim 29 (Withdrawn) The method of Claim 28 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

Claim 30 (Withdrawn) The method of Claim 28 wherein said semiconductor substrate includes a trench isolation region and said at least one resistor is formed thereon.

Claim 31 (Withdrawn) The method of Claim 28 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, or SiCr.

Claim 32 (Withdrawn) The method of Claim 31 wherein said conductive metal comprises TiN, TaN, NiCr or SiCr.

Claim 33 (Withdrawn) The method of Claim 28 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 34 (Withdrawn) The method of Claim 28 wherein said planarized dielectric material comprising an oxide.

Claim 35 (Withdrawn) A method for integrating a metal resistor into a CMOS technology comprising the steps of:

providing a structure including at least one FEOL device located on a surface of a semiconductor substrate;

forming a silicide metal layer over said structure;

forming a dielectric material over said silicide metal layer;

patterning said dielectric material to provide at least one stack of a patterned dielectric material atop a portion of said silicide metal layer, said at least one stack is located atop said surface of said semiconductor substrate;

siliciding to convert at least the silicide metal layer of said stack into a metal silicide, wherein said metal silicide of said stack comprises a conductor of a resistor; and

forming a first level of metallization over at least said stack and said at least one FEOL device.

Claim 36 (Withdrawn) The method of Claim 35 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

Claim 37 (Withdrawn) The method of Claim 35 wherein said silicide metal layer comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

Claim 38 (Withdrawn) The method of Claim 35 wherein said siliciding comprising a first anneal that performed at a temperature from about 300° to about 600°C

Claim 39 (Withdrawn) The method of Claim 38 wherein following said first anneal a wet etch process is employed removed to selectively remove unreacted silicide metal layer.

Claim 40 (Withdrawn) The method of Claim 39 further comprising a second anneal as part of said siliciding, said second anneal is performed at a temperature from about 600° to about 800°C.